REMARKS

In the Office Action, the Examiner rejected claims 1, 4-9, 15-22, 28-32, 36-40, and 44 under 35 U.S.C. § 102(b) as anticipated by Wang (U.S. Patent No. 5,563,891); rejected claims 2, 3, 10, and 23 under 35 U.S.C. § 103(a) as unpatentable over Wang in view of Co et al. (U.S. Patent No. 5,602,882); and rejected claims 11-14, 24-27, 33-35, and 41-43 under 35 U.S.C. § 103(a) as unpatentable over Wang in view of Mays et al. (U.S. Patent No. 5,384,770).

By this Amendment, Applicants amend claims 1, 5, 9, 13-16, 18, 22-26, 28, 29, and 35-37 to improve form. Applicants also add new claim 45. Applicants respectfully traverse the Examiner's rejections under 35 U.S.C. §§ 102 and 103 with regard to the claims as amended herein. Claims 1-45 are pending.

In paragraph 2 of the Office Action, the Examiner rejected claims 1, 4-9, 15-22, 28-32, 36-40, and 44 under 35 U.S.C. § 102(b) as allegedly anticipated by Wang. Applicants respectfully traverse the rejection.

Amended claim 1 recites a combination of features of a system for reliably receiving data. The system includes a memory, write logic, and read logic. The write logic is configured to receive data and an unreliable clock signal and write the data to the memory using the unreliable clock signal. The read logic is configured to generate a data enable signal and a gapped clock signal and read the data from the memory using the data enable signal and a constant local clock signal. The gapped clock signal is generated by turning on and off the constant local clock signal.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught

must be inherently present. In other words, the identical invention must be shown in as complete detail as contained in the claim. See M.P.E.P. § 2131. Wang does not disclose or suggest the features recited in amended claim 1. For example, Wang does not disclose or suggest read logic that is configured to generate a data enable signal and a gapped clock signal and read the data from the memory using the data enable signal and a constant local clock signal, where the gapped clock signal is generated by turning on and off the constant local clock signal. Instead, Wang discloses reading data from memory using a gapped read clock (Fig. 3; col. 2, lines 47-60). Wang does not disclose or suggest reading data from memory using a data enable signal and a constant local clock signal, as recited in amended claim 1.

For at least these reasons, Applicants submit that claim 1 is not anticipated by Wang. Claims 4-9 depend from claim 1 and are, therefore, not anticipated by Wang for at least the reasons given with regard to claim 1. Moreover, claims 4-9 are also not anticipated by Wang for reasons of their own.

For example, amended claim 5 recites a first state machine that is configured to generate an enable signal having at least two states and the data enable signal, and a second state machine that is configured to turn on and off the constant local clock signal based on the state of the enable signal to generate the gapped clock signal. Wang does not disclose or suggest these features.

For example, Wang does not disclose or suggest a first state machine that generates an enable signal that has at least two states and the data enable signal. The Examiner alleged that Wang discloses a first state machine and pointed to justification decision circuit 635 of Wang for support (Office Action, page 3). Applicants disagree. Wang discloses that justification decision

circuit 635 compares the phase difference signal outputted by comparison circuit 630 to a threshold and outputs a justification signal that includes pulses that correspond to instances in which the phase difference signal exceeds the threshold (Fig. 4(c); col. 3, lines 39-52). Wang does not disclose or suggest that justification decision circuit 635 generates a data enable signal and an enable signal that has at least two states, as recited in amended claim 5.

For at least these additional reasons, Applicants submit that claim 5 is not anticipated by Wang.

Amended claim 9 recites, among other things, that the read logic is configured to compensate for underflow conditions in the memory by turning off the constant local clock signal and disabling the data enable signal. Wang does not disclose or suggest these features. For example, Wang does not disclose read logic that compensates for underflow conditions in the memory by disabling a data enable signal. In fact, Wang does not disclose a data enable signal that is used to read data from memory.

For at least these additional reasons, Applicants submit that claim 9 is not anticipated by Wang.

Amended claim 15 recites a combination of features of a system for reliably receiving data. The system includes means for receiving data and an unreliable clock signal, means for writing the data to a memory using the unreliable clock signal, means for generating a reliable clock signal by turning on and off a local clock signal, means for generating a data enable signal, and means for reading the data from the memory using the data enable signal and the local clock signal.

Wang does not disclose or suggest these features. For example, Wang does not disclose or suggest means for generating a data enable signal or means for reading the data from the memory using the data enable signal and a local clock signal that is used for generating a reliable clock signal. Instead, Wang discloses that data is read from memory using a gapped read clock (Fig. 3; col. 2, lines 47-60).

For at least these reasons, Applicants submit that claim 15 is not anticipated by Wang.

Amended claims 16 and 28 recite features similar to features recited in claim 15. Claims 16 and 28 are, therefore, not anticipated by Wang for reasons similar to those given with regard to claim 15. Claims 17-22, 29-32, and 36 variously depend from claims 16 and 28 and are, therefore, not anticipated by Wang for at least the reasons given with regard to claims 16 and 28. Claims 17-22, 29-32, and 36 also recite features similar to features recited in claims 4-9. Claims 17-22, 29-32, and 36 are, therefore, also not anticipated by Wang for reasons similar to those given with regard to claims 4-9.

Amended claim 37 recites a combination of features of a clock generator that includes first and second state machines. The first state machine is configured to enter a plurality of states based, at least in part, on whether a memory stores data. Within certain ones of the states, the first state machine is configured to generate first and second enable signals, where the first enable signal is used to read data from the memory that was written to the memory using an unreliable clock signal. The second state machine is configured to enter a plurality of states based, at least in part, on the second enable signal. Within one of the states, the second state machine is configured to generate a gapped clock signal for reliably recovering the data. Within another one of the states, the second machine is configured to generate no gapped clock signal.

Wang does not disclose or suggest these features. For example, Wang does not disclose or suggest a first state machine that is configured to enter a plurality of states based, at least in part, on whether a memory stores data, where within certain ones of the states, the first state machine is configured to generate first and second enable signals, and where the first enable signal is used to read data from the memory that was written to the memory using an unreliable clock signal.

The Examiner alleged that Wang discloses a first state machine and appears to be identifying multiplexer 650 and justification decision circuit 635 of Wang as corresponding to the first state machine (Office Action, page 5). The Examiner also alleged that the frame timing signal corresponds to the first enable signal and the justification signal corresponds to the second enable signal (Office Action, page 5). Applicants disagree.

Wang discloses that multiplexer 650 generates a frame timing signal that is high during payload and stuffing bit positions of the channel of the higher rate signal corresponding to the lower rate signal and low at other times (col. 3, lines 57-62). Wang discloses that justification decision circuit 635 compares the phase difference signal outputted by comparison circuit 630 to a threshold and outputs a justification signal that includes pulses that correspond to instances in which the phase difference signal exceeds the threshold (Fig. 4(c); col. 3, lines 39-52). Nowhere does Wang disclose or suggest that multiplexer 650 and/or justification decision circuit 635 enter a plurality of states based, at least in part, on whether a memory stores data. Wang also does not disclose that within certain ones of the states, multiplexer 650 and/or justification decision circuit 635 generate first and second enable signals, where the first enable signal is used to read data from the memory that was written to the memory using an unreliable clock signal.

Wang also does not disclose or suggest a second state machine that is configured to enter a plurality of states based, at least in part, on the second enable signal, where within one of the states, the second state machine is configured to generate a gapped clock signal for reliably recovering the data, and within another one of the states, the second machine is configured to generate no gapped clock signal, as required by claim 37. The Examiner identified logic circuit 645 as allegedly corresponding to the second state machine (Office Action, page 5). Applicants disagree.

Wang discloses that logic circuit 645 corresponds to an AND gate that outputs a gapped read clock from a combination of a local oscillator clock, a frame timing signal, and a justification signal, where the gapped read clock is used to read data from memory (Fig. 3; col. 2, lines 47-60; col. 3, lines 53-66). Nowhere does Wang disclose that logic circuit 645 enters a plurality of states in which it generates or does not generate a gapped clock signal, based, at least in part, on a second enable signal.

For at least these reasons, Applicants submit that claim 37 is not anticipated by Wang. Claims 38-40 and 44 depend from claim 37 and are, therefore, not anticipated by Wang for at least the reasons given with regard to claim 37.

In paragraph 3 of the Office Action, the Examiner rejected claims 2, 3, 10, and 23 under 35 U.S.C. § 103(a) as allegedly unpatentable over Wang in view of Co et al. Applicants respectfully traverse the rejection.

Claims 2, 3, 10, and 23 variously depend from claims 1 and 16. The disclosure of Co et al. fails to cure the deficiencies in the disclosure of Wang as noted above with regard to claims 1 and 16. Claims 2, 3, 10, and 23 are, therefore, patentable over Wang and Co et al., whether taken

alone or in any reasonable combination, for at least the reasons given with regard to claims 1 and 16. Claims 2, 3, 10, and 23 are further patentable for reasons of their own.

For example, with regard to claim 3, the Examiner alleged that Co et al. discloses a first-in, first-out memory (Office Action, page 6). To establish a prima facie case of obviousness under 35 U.S.C. § 103 based on a combination of references, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the teachings of the references (M.P.E.P. § 2143). According to M.P.E.P. § 2143, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In this case, the Examiner provided absolutely no motivation for adding the alleged first-in, first-out memory of Co et al. to the system of Wang. For at least these reasons, the Examiner's rejection is improper and should be withdrawn.

With regard to claim 10, the Examiner alleged that Co et al. discloses generating a data error when overflow conditions occur (Office Action, page 6). Again, the Examiner provided absolutely no motivation for adding the alleged "generating a data error when overflow conditions occur" of Co et al. to the system of Wang. For at least these reasons, the Examiner's rejection is improper and should be withdrawn.

Similar deficiencies exist in the Examiner's rejection of claim 23. In other words, the Examiner provided no motivation for combining the alleged features of Co et al. and Wang. For at least these reasons, the Examiner's rejection is improper and should be withdrawn.

In paragraph 4 of the Office Action, the Examiner rejected claims 11-14, 24-27, 33-35, and 41-43 under 35 U.S.C. § 103(a) as allegedly unpatentable over Wang in view of Mays et al. Applicants respectfully traverse the rejection.

Claims 11-14, 24-27, 33-35, and 41-43 variously depend from claims 1, 16, 28, and 37. The disclosure of Mays et al. fails to cure the deficiencies in the disclosure of Wang as noted above with regard to claims 1, 16, 28, and 37. Claims 11-14, 24-27, 33-35, and 41-43 are, therefore, patentable over Wang and Mays et al., whether taken alone or in any reasonable combination, for at least the reasons given with regard to claims 1, 16, 28, and 37. Claims 11-14, 24-27, 33-35, and 41-43 are further patentable for reasons of their own.

For example, with regard to claim 12, the Examiner alleged that Mays et al. discloses determining that write logic has received data before a counter reaches a predetermined count (Office Action, page 7). Again, the Examiner provided absolutely no motivation for adding the alleged "determining that write logic has received data before a counter reaches a predetermined count" of Mays et al. to the system of Wang. For at least these reasons, the Examiner's rejection is improper and should be withdrawn.

With regard to claims 13 and 14, the Examiner alleged that Mays et al. discloses determining that the counter has reached a predetermined count (Office Action, page 7). Again, the Examiner provided absolutely no motivation for adding the alleged "determining that the counter has reached a predetermined count" of Mays et al. to the system of Wang. For at least these reasons, the Examiner's rejections are improper and should be withdrawn.

Similar deficiencies exist in the Examiner's rejections of claims 24-27, 33-35, and 41-43. In other words, the Examiner provided no motivation for combining the various alleged features

of Mays et al. and Wang. For at least these reasons, the Examiner's rejections are improper and should be withdrawn.

New claim 45 recites a combination of features of a system that includes a memory, write logic, and read logic. The write logic is configured to receive data and an unreliable clock signal and write the data to the memory using the unreliable clock signal. The read logic includes first and second state machines. The first state machine is configured to enter a plurality of states based, at least in part, on whether the memory stores data. Within certain ones of the states, the first state machine is configured to generate first and second enable signals. The first enable signal is used to read data from the memory. The second state machine is configured to enter a plurality of states based, at least in part, on the second enable signal. Within one of the states, the second state machine is configured to generate a gapped clock signal for reliably recovering the data. Within another one of the states, the second machine is configured to generate no gapped clock signal.

None of the references applied by the Examiner, whether taken alone or in any reasonable combination, discloses or suggests the features of new claim 45. For example, none of the references discloses the features of the first and second state machines. For at least these reasons, Applicants submit that new claim 45 is patentable over the applied references, whether taken alone or in any reasonable combination.

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and allowance of pending claims 1-45.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

HARRITY & SNYDER, L.L.P

By: 
Paul A. Harrity
Reg. No. 39,574

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11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
571-432-0800